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FIG. 2 PRIOR ART

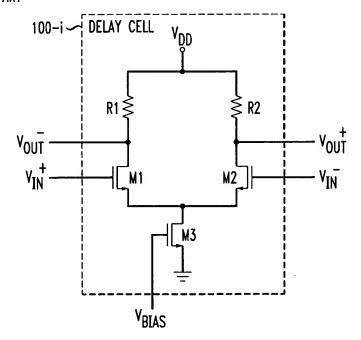
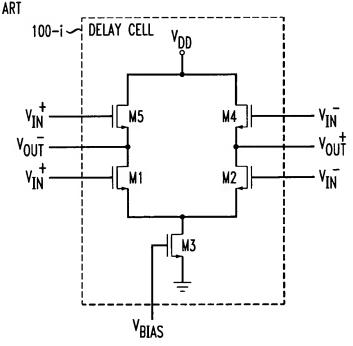
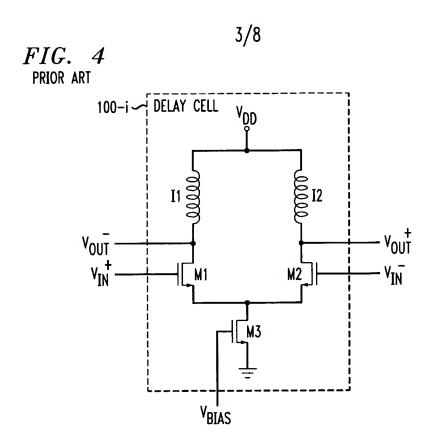


FIG.~3 prior art





PRIOR ART

100-i DELAY CELL

VDD

I1 DELAY CELL

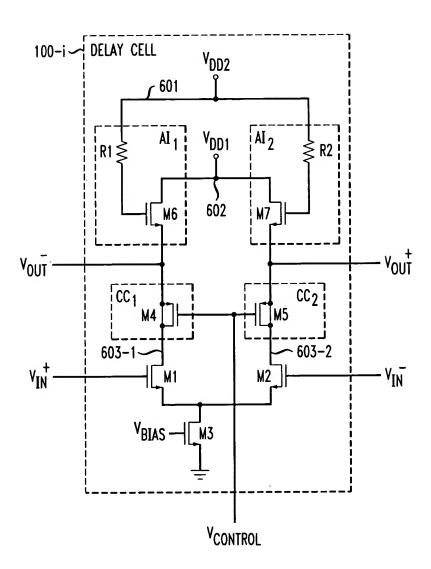
VDD

VCONTROL

VBIAS

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FIG. 6



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FIG. 7a

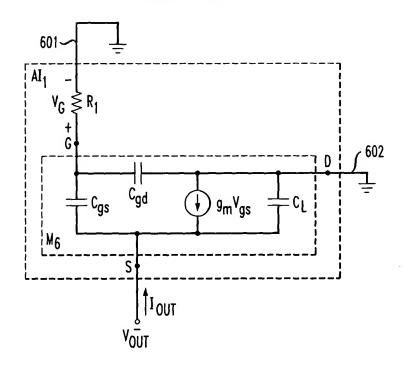
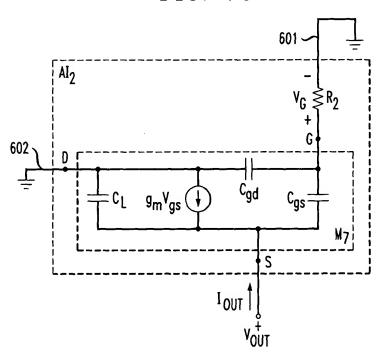
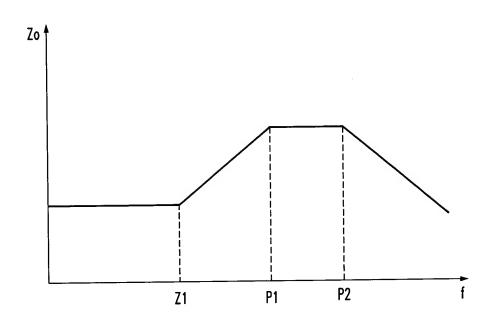


FIG. 7b

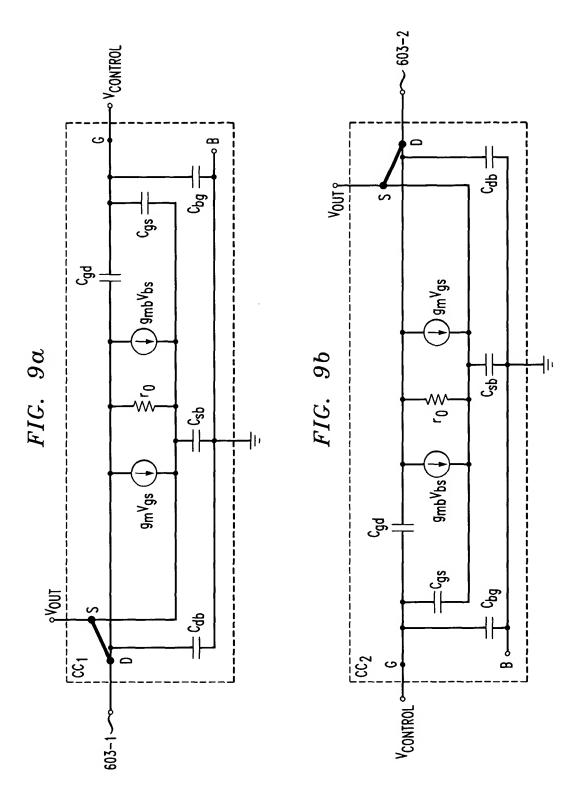


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FIG. 8



GRAPH OF Zo VERSUS FREQUENCY



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FIG. 9c

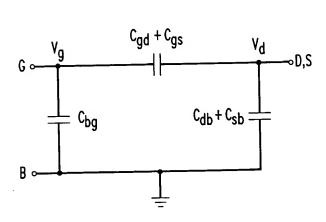


FIG. 9d

